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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,872	09/16/2003	Vladimir M. Stojanovic	57941.000025	1169

38013 7590 07/13/2006

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EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,872	STOJANOVIC ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-171* is/are pending in the application.

4a) Of the above claim(s) *89-105,110-141 and 148-171* is/are withdrawn from consideration.

5)☒ Claim(s) *53-71* is/are allowed.

6)☒ Claim(s) *1-19,30-40,42-45,48-52,72-74,76,80-88,106-109 and 142-147* is/are rejected.

7)☒ Claim(s) *20-29,41,46,47,75 and 77-79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-88, 106-109, and 142-147 in the reply filed on 5/4/2006 is acknowledged. The traversal is on the ground(s) that the inventions are related and not independent from each other. This is not found persuasive because MPEP 803, Section I, states there are two criteria for a proper requirement for restriction between patentably distinct inventions:

(A) The inventions must be independent (see MPEP § 802.01, § *>806.06<, § 808.01) or distinct as claimed (see MPEP § 806.05 - § *>806.05(j)<); and

(B) There *>would< be a serious burden on the examiner if restriction is >not< required (see MPEP § 803.02, **> § 808<, and § 808.02).

Therefore, although the inventions are not independent, the MPEP states that as long as the inventions are distinct, a restriction is proper.

MPEP 802.1 [R-3], Section II defines the term "**distinct**" as the following:

****> Two or more inventions are related (i.e., not independent) if they are disclosed as connected in at least one of design (e.g., structure or method of manufacture), operation (e.g., function or method of use), or effect. Examples of related inventions include< combination and part (subcombination) thereof, process and apparatus for its practice, process and product made, etc. **>In< this definition the term related is used as an alternative for dependent in referring to *>inventions< other than independent**

>inventions<.> Related inventions are distinct if the inventions as claimed are not connected in at least one of design, operation, or effect (e.g., can be made by, or used in, a materially different process) and wherein at least one invention is PATENTABLE (novel and nonobvious) OVER THE OTHER (though they may each be unpatentable over the prior art). See MPEP § 806.05(c) (combination and subcombination) and § 806.05(j) (related products or related processes) for examples of when a two-way test is required for distinctness.<

Therefore, from the above definition inventions which are related may also be patentably distinct with regard to each other which would make restriction proper. In the instant case, Invention I (Claims 1-88, 106-109, and 142-147) refers to an equalizer in a receiver which generates samples on an input signal based on a threshold value and selects one of the samples to be used to generate an equalization signal. Invention II (Claims 89-105 and 110-141) refers to a data clock recovery circuit which adjusts the phase of a clock signal according to the state of a sample of the input data signal. Invention III (148-171) refers to a differential amplifier receiver including a plurality of differential amplifiers and resistive elements which draw currents through the resistive elements according to signal levels of the input signal. Although these inventions are related to a receiver, the above definition of "distinct" states "Related inventions are distinct if the inventions as claimed are not connected in at least one of design, operation, or effect (e.g., can be made by, or used in, a materially different process) and wherein at least one invention is PATENTABLE (novel and nonobvious) OVER THE OTHER." The above claimed inventions are not connected in operation (Invention I equalizes a signal, Invention II recovers a clock signal, and Invention III draws currents from differential signals) and are also patentable

over each other (though they may each be unpatentable over the prior art). Because of the different operation and classification as explained in the Office Action mailed 4/5/2006, the inventions require a different field of search (see MPEP § 808.02), thus, restriction for examination purposes as indicated is proper and thus made final.

Claim Objections

2. Claims 19 and 42-52 are objected to because of the following informalities:

a. In claim 19, line 1, the phrase "wherein signal" is suggested to be changed to "wherein the signal".

b. In claim 42, line 5, the phrase " a second pair of the signal" is suggested to be changed to "a second pair of samples of the signal". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12, 19, 30-34, 37, 42-45, 48, 50, and 142-144 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071).

Regarding claim 1, Gitlin et al. discloses a detector/non-linear canceller which can be implemented as an integrated circuit device (see Fig. 5, column 11, lines 48-50) for receiving a signal transmitted via an optical fiber (see column 2, lines 28-35), the integrated circuit device comprising:

a first comparator (Fig. 5, block 511) to generate a first decision value (Aj) that indicates whether the signal exceeds a first threshold level known as V1 (see column 6, line 64-column 7, line 10);

a second comparator (Fig. 5, block 512) to generate a second decision value (Bj) that indicates whether the signal exceeds a second threshold level known as V2 (see column 6, line 64-column 7, line 10); and

a mux circuit (Fig. 5, block 541) coupled to receive the first and second values (Aj and Bj) from the first and second comparators and configured to select as described in column 7, lines 10-20, according to an immediate previously generated decision value (aj-1), either the first (bit) value or the second (bit) value to be output as a selected value on the output lead 39.

Gitlin et al. does not specifically disclose the first and second comparators are sampling circuits which compare samples to the threshold values to generate sample values. However, Gitlin et al. does disclose the comparators can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Popplewell et al. further discloses sampling an input signal regular

intervals and a threshold slicer which selects an ideal sample by comparing sampled values with received thresholds (see Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of Gitlin et al. to compare samples with the thresholds as taught by Popplewell et al. and use different phase timing for the sampling clocks since Gitlin et al. states that the comparators can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Regarding claim 2, Gitlin et al. further discloses a flip flop (Fig. 5, block 551) representing a first storage circuit to store the immediate previously generated value (wherein the output of flip flop 551 is aj-1) , the first storage circuit having an output (aj-1) coupled to a select input of the mux (Fig. 5, block 541) representing the first select circuit to output the immediate previously generated sample thereto as described in column 7, lines 17-20).

Regarding claim 3, Gitlin et al. discloses the flip flop circuit (Fig. 5, block 551) has a data input (D) coupled to the mux (Fig. 1, block 541) to receive the selected value and a clock input (where the clock is in input on component 551 of Fig. 5) to receive a first clock signal, the first storage circuit being configured to store (input) the value in response to a transition of a first clock cycle as described in column 6, line 66-column 7, line 5.

Regarding claim 4, Gitlin et al. discloses the selected value, when stored in the first storage circuit, constitutes the immediate previously generated value (aj-1) of the first clock phase in relation to a subsequent pair of values (see column 7, lines 10-20) generated by the first and second comparator circuits in a second clock phase, one of which will be selected using the value generated in the first clock phase as described in column 7, line 10-20.

Regarding claim 5, Gitlin et al. disclosed the immeadiate previously generated value (aj-1) is generated by one of the first and second comparator circuits and held (column 7, lines 10-12) prior to generation of the first decsion value and the second decision value.

Regarding claim 6, Gitlin et al. further discloses:

a third comparator (Fig. 5, block 513) to generate a third value (Cj) that indicates whether the signal exceeds a threshold level (V3); and

a fourth comparator (Fig. 5, block 514) to generate a fourth value (Dj) that indicates whether the signal exceeds a threshold level (V4).

However, Gitlin et al. does not specifically disclose threshold levels are the first and second threshold levels applied to the first and second comparator. However, Gitlin et al. does disclose that similar multiple detectors/cancellers can be combined to determine which bits of a sequence where most likely transmitted to a receiver (see column 11, lines 34-40). Thus, it is the understanding to the examiner, that in order to determine which bits were most likely received, different bits of a sequence would be applied to comparators of multiple detectors with the same thresholds to determine bit (tentative) decisions for each bit as described in column 7, lines 5-20. Therefore, claim 6 is rejected over the teachings of Gitlin et al. in view of Popplewell et al. as explained above

Regarding claim 7, Gitlin et al. discloses a mux (Fig. 5, block 542) representing a second select circuit coupled to receive the third and fourth values (Cj and Dj) from the third and fourth comparator circuits (Fig. 5, block 513 and 514), the second select circuit being configured to select either the third value or the fourth value to be stored (if selected by mux 543) in the first

storage circuit (Fig. 5, block 551) as the previously generated sample value (aj-1), wherein the second select circuit functions in the same manner as the first select circuit described in claim 1.

Regarding claim 8, Gitlin et al. discloses the comparator circuits can operate using clock signals with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20).

Regarding claim 9, Gitlin et al. discloses the comparator circuits can operate using clock signals with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Operating the comparator circuits using different clock signals would produce values at different times, which allows for better distortion compensation according to Gitlin et al. (see column 9, lines 13-20).

Regarding claim 10, Gitlin et al. discloses the comparator circuits can operate using clock signals with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Operating the comparator circuits using different clock signals such as phase offsets of half-cycles would produce values at different times, which allow for better distortion compensation according to Gitlin et al. (see column 9, lines 13-20).

Regarding claim 11, Gitlin et al. discloses the first comparator compares the signal with a first threshold voltage signal level (V1, wherein V=voltage) to determine whether the signal exceeds the first threshold level (see column 6, line 57-column 7, line 5).

Regarding claim 12, Gitlin et al. discloses a threshold generating circuit (Fig. 4, block 438) to generate the first threshold voltage signal level (see column 6, lines 57-60).

Regarding claim 19, Gitlin et al. further discloses the received is a multi-level signal (column 11, lines 14-21), wherein multi-level signals are representative of more than a single binary bit (bi-level) and wherein the first sample value generated by the first sampling circuit can comprise more than one binary bit if multi-level signaling is used as disclosed by Gitlin et al. (wherein bit decisions would comprise of more than one bit because of multi-level signaling.

Regarding claim 30, Gitlin et al. discloses a method of operation within a detector/non-linear canceller implemented in an integrated circuit device (Fig. 5, column 11, lines 48-50), the method comprising:

receiving a data signal from an external optical fiber (column 2, lines 28-35);

generating (Fig. 5, block 511, column 6, line 64-column 7, line 5) a first data value (Aj) having one of at least two states (0 or 1) according to whether the data signal exceeds a first threshold level (V1);

generating (Fig. 5, block 512, column 6, line 64-column 7, line 5) a second data value (Bj) having one of the at least two states (0 or 1) according to whether the data signal exceeds a second threshold level (V2); and

selecting using a mux (Fig. 5, block 541) either the first data value (Aj) or the second data value (Bj) to be a selected value (bit decision) of the data signal on output lead 39 of Fig. 5 as described in column 7, lines 10-20.

Gitlin et al. does not specifically disclose the generated values are samples. However, Gitlin et al. does disclose the comparators used to generate the data values can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Popplewell et al. further discloses

sampling an input signal regular intervals and a threshold slicer which selects an ideal sample by comparing sampled values with received thresholds (see Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of Gitlin et al. to generate and compare samples with the thresholds as taught by Popplewell et al. and use different phase timing for the sampling clocks since Gitlin et al. states that the comparators used to generate the data values can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Regarding claim 31, Giltin et al. discloses selecting either the first data value or the second data value to be the selected value comprises selecting either the first data value (Aj) or the second data value (Bj) as the bit (tentative) decision according to whether a third data value (aj-1) has a first state or a second state (0 or 1) as disclosed in column 7, lines 10-20

Regarding claim 32, Gitlin et al. discloses generating the third data value (aj-1) immediately prior to generating the first and second data values (see column 7, lines 10-20).

Regarding claim 33, Gitlin et al. discloses generating a first data value comprises generating a first data value having one of two binary states (0 or 1) according to whether the data signal exceeds a first threshold (V1) as described in column 6, line 64-column 7, line 5.

Regarding claim 34, Gitlin et al. and Popplewell et al. do not specifically disclose generating a first data value comprises generating a first data value having one of more than two possible states. However, Gitlen et al. does disclose multi-level signal could be used (see column 11, lines 14-21), wherein more than one bit is used to represent data. Thus, since the first decision (data) value corresponding to a multi-level signal would include more than one bit

such as 00, the first (data) decision value could have more that two possible states such as 00, 01, 11, or 10 when multi-level signaling is used.

Regarding claim 37, Gitlin et al. further discloses

determining a first voltage level of the data signal by subtracting the known reference voltage (V1) from the data signal using subtracter 436 of Fig. 4 to create an error signal as described in column 3, lines 25-35;

determining a second voltage level of the data signal by subtracting the known reference voltage (V2) from the data signal using subtracter 440 of Fig. 4 to create an error signal as described in column 3, lines 25-35; and

generating the first threshold level by updating threshold levels using the error signals in update circuitry 437 as described in column 5, lines 35-47 wherein the error signal represent the error between the first and second voltage levels of the data signal and the reference voltages as described in column 3, lines 25-35.

Regarding claim 42, Gitlin et al. discloses detector/non-linear canceller implemented in an integrated circuit device (Fig. 5, column 11, lines 48-50) for receiving a signal transmitted via an electric signal conductor such as an optical fiber (see column 2, lines 28-35), the integrated circuit device comprising:

a first pair of comparator circuits (Fig. 5, blocks 511 and 512) to capture a first pair of data (decision) values (0 or 1) of the signal (see column 4, line 64-column 7, line 10) in response to a first clock signal applied to the comparators as described in column 9, lines 13-20;

a second pair of comparator circuits (Fig. 5, blocks 513 and 514) to capture a second pair of decision values as described in column 4, line 64-column 7, line 10 of the signal in response to

a second clock signal which can be different in phase timings from the first clock signals as described in column 9, lines 13-20); and

a first select circuit (Fig. 5, block 541) coupled to the first pair of comparator circuits and configured to select one decision value of the first pair of values (see column 7, lines 10-20) according to a state of a selected value output from mux 542 of Fig. 5 of the second pair of samples, wherein the value (aj-1) used to determine the selection from the first select (mux) circuit is based on the state of the selected value output from the second mux 542 which is applied to mux 543 to determine the value aj-1 as shown in Fig. 5.

Gitlin et al. does not specifically disclose the comparators are sampling circuits which compare samples to the threshold values to generate sample values. However, Gitlin et al. does disclose the comparators can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Popplewell et al. further discloses sampling an input signal regular intervals and a threshold slicer which selects an ideal sample by comparing sampled values with received thresholds (see Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of Gitlin et al. to compare samples with the thresholds as taught by Popplewell et al. as use different phase timing for the sampling clocks since Gitlin et al. states that the comparators can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Regarding claim 43, Gitlin et al. further discloses a second select circuit (Fig. 5, block 542) coupled to the second pair of comparator circuits (block 513 and 514) to select the selected value of the second pair of samples.

Regarding claim 44, Gitlin et al discloses a flip flop representing a first storage circuit (Fig. 5, block 551) coupled to receive the one value of the first pair of values from the first select circuit when the value is also selected by mux 543 of Fig. 5 and configured to store the one value of the first pair of values in response to a clock cycle as described in column 6, line 64-column 7, line 5.

Regarding claim 45, Gitlin et al. disclose an output (aj-1) of the first storage circuit (Fig. 5, block 551) is coupled to a select input of the second select (mux) circuit (Fig. 5, block 542) such that the state of value stored in the first storage circuit determines which value of the second pair of samples is selected by the second select circuit as described in column 7, lines 10-20.

Regarding claim 48, Gitlin et al. discloses the comparator circuits can operate using clock signals with different phase timings (offsets) so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Operating the comparator circuits using different clock signals such as phase offsets of half-cycles would produce values at different times, which allow for better distortion compensation according to Gitlin et al. (see column 9, lines 13-20).

Regarding claim 50, Gitlin et al. discloses a first comparator (Fig. 5, block 511) of the first pair of comparator circuits is configured to determine whether the signal exceeds a first threshold level (V1) (see column 6, line 64-column 7, line 10), and wherein a second comparator

circuit of the first pair of comparator circuits is configured to determine whether the signal exceeds a second threshold level (V2).

Regarding claim 142, Gitlin et al. discloses a method of operation within a signaling system (Fig. 4 and Fig. 5), the method comprising:

outputting a sequence of data values (symbols) onto an electric signal conductor such as a optical fiber (column 2, lines 28-35) during successive transmission intervals, the sequence of data values forming a data signal on the electric signal conductor;

generating, during each of a sequence of data reception intervals (symbol periods), a first decision value (Aj) having either a first state or second state (0 or 1) according to whether a signal level of the electric signal conductor exceeds a first threshold level (V1) as described in column 6, line 64-column 7, line 10) and a second decision value (Bj) having either the first state or second state (0 or 1) according to whether the signal level exceeds a second threshold level (V2), see also column 6, line 64-column 7, line 10); and

selecting using a mux (Fig. 4, block 439), during each of the data reception intervals after a first one of the data reception intervals, either the first decision value or the second decision value (see column 7, lines 8-16) to be a received data bit value according to the state of at least one received data bit value (aj-1) selected at an immediate prior reception interval.

Gitlin et al. does not specifically disclose the generated decision values are samples. However, Gitlin et al. does disclose the comparators used to generate the decision values can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Popplewell et al. further discloses sampling an input signal regular intervals and a threshold slicer which selects an

ideal sample by comparing sampled values with received thresholds (see Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of Gitlin et al. to generate and compare samples with the thresholds as taught by Popplewell et al. and use different phase timing for the sampling clocks since Gitlin et al. states that the comparators used to generate the data values can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Regarding claim 143, Gitlin et al. discloses selecting either the first decision value (Aj) or the second decision value (Bj) to be the received data bit value comprises selecting either the first decision value (Aj) or the second decision value (Bj) to be the received data bit value (see column 7, lines 5-16) according to the state of a received data bit decision value (aj-1) selected during an immediately preceding one of the reception intervals as described in column 7, lines 5-16).

Regarding claim 144, Giltin et al. discloses selecting, during one of the data reception intervals (symbol periods), either the first decision value or the second decision value to be the received data bit value (see column 7, lines 5-16) according to the state of a bit decision value (aj-1) selected during a reception interval immediately preceding the current data reception (column 7, lines 9-15).

5. Claims 13-18, 35, 36 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071) as applied to claims 1, 30, and 42, and in further view of Fernandez et al. (U. S. Patent No. 5, 448, 200).

Regarding claims 13 and 14, Gitlin et al. and Popplewell do not disclose the received signal is a differential signal or a comparator to compare the differential signal against a threshold level.

However, Fernandez et al. discloses a differential comparator (Fig. 1) which receives and compares a differential signal (IN+ and IN-) to a threshold level (A) and outputs a value (OUT+ and OUT-) based on the comparison (see column 2, line 59-column 3, line 6). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the comparators of Gitlin et al. and Popplewell et al. to receive differential signals as taught by Fernandez et al. since Fernandez et al. states a fully differential receiver increases the robustness of a receiver which receives signals from wires (column 1, lines 40-41).

Regarding claim 15, Fernandez et al. discloses creating a threshold level exceeding the common mode of a differential signal to detect differential signals (column 1, lines 50-56). It would have been obvious to include this feature since Fernandez et al. states accepting signals above this threshold as data rejects noise (column 1, lines 50-56).

Regarding claims 16-18, Gitlin et al., Popplewell et al., and Fernandez et al. do not specifically disclose a common mode of the differential signal exceeds the second threshold level, the common mode of the differential signal is substantially centered between the first and second threshold levels, or the first threshold level exceeds the common mode of the differential signal by a voltage that corresponds to a level of inter-symbol interference produced by at least one prior signal transmission on the electric signal transmission. However, Fernandez et al. discloses creating a threshold level exceeding the common mode of a differential signal to detect differential signals (column 1, lines 50-56). Common mode signals include noise which can

interfere with the signal (column 1, lines 44-50). Therefore, it would have been obvious to create proper thresholds for detecting common mode signals of the differential signals since Fernandez et al. states creating proper thresholds to detect common mode signals rejects noise (column 1, lines 50-56).

Regarding claim 35, the claimed method includes features corresponding to the above rejection of claims 15 and 16, which is applicable hereto.

Regarding claim 36, the claimed method includes features corresponding to the above rejection of claim 17, which is applicable hereto.

Regarding claim 49, Gitlin et al. and Popplewell et al. do not disclose the received signal is a differential signal and each sampling (comparator) circuit is a differential sampling circuit.

However, Fernandez et al. discloses a differential comparator (Fig. 1) which receives and compares a differential signal (IN+ and IN-) to a threshold level (A) and outputs a value (OUT+ and OUT-) based on the comparison (see column 2, line 59-column 3, line 6). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the comparators (samplers) of Gitlin et al. and Popplewell et al. to receive differential signals as taught by Fernandez et al. and create differential samples since Fernandez et al. states a fully differential receiver increases the robustness of a receiver which receives signals from wires (column 1, lines 40-41).

6. Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071) as applied to claim 30, and in further view of Kasturia et al. "Adaptive Nonlinear Cancellation for

High-Speed Fiber-Optic Systems, Journal of Lightwave Technology, Volume 10, Issue 7, July 1992 Page(s):971 – 977.

Regarding claims 38-40, Gitlin et al. discloses generating a control value (wherein it is the understanding of the examiner that this value can be digital to ease implementation problems, see column 6, lines 44-56) to update the reference signals (voltages) (column 5, lines 41-43) used to adjust the threshold levels (column 5, lines 25-35). Gitlin et al. and Popplewell do not disclose this updating is performed averaging values representative of the first and second voltage levels of the received data signal.

However, Kasturia et al. discloses a nonlinear cancellation system similar to that of Gitlin et al. and Popplewell et al. which generates values by comparing a received signal to threshold values (see Fig. 7). Kasturia et al. further discloses determining the threshold values by averaging the estimated signal (voltage) levels (see page 974, column 2, paragraph 2). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Gitlin et al. and Popplewell et al. with the teachings of Kasturia et al. since Kasturai et al. states using the average (median) signal level to adjust acquisition (detection) thresholds decreases bit error rate (see page 973, paragraph 3).

7. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071) as applied to claim 42, and in further view of Hui (U. S. Patent No. 6, 262, 591).

Regarding claims 51 and 52, Gitlin et and Popplewell et al. do not disclose the signal is a differential signal having a first common mode level when at a steady state, and wherein the first common mode level is lower than the first threshold level and above the second threshold level

and the first common mode level is substantially centered between the first and second threshold levels.

However, Hui discloses a differential receiver (Fig. 2, block 24), wherein the common mode voltage is equal to a centered threshold voltage centered between a first threshold (logic "1") and a second threshold (logic "0") used to detect differential signals, see column 4, lines 30-34 and 44-47. Therefore, it would have been obvious to incorporate a differential receiver in Gitlin et al. and Popplewell et al. as described by Hui since a fully differential receiver increases the robustness of a receiver which receives signals from wires (see rejection above) and maintaining a balanced threshold voltage (common mode voltage) obtains maximum noise tolerance (see Hui, column 2, lines 57-59).

8. Claims 72-74, 76, 80-88, 106-109 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071) and in further view of Darabi et al. (U. S. Patent No. 6, 970, 681).

Regarding claim 72, Gitlin et al. discloses a method of operating a detector/non-linear canceller within an integrated circuit device (see Fig. 5,column 11, lines 48-50), the method comprising:

generating first and second decision values (Aj and Bj) using comparators (Fig. 4, blocks 431 and 432) of an input data signal (see column 6, line 64-column 7, line 5), each value having either a first state (0) or a second state (1) according to whether the input data signal exceeds a respective one of first (V1) and second threshold levels (V2);

generating a first received data value (current bit value) based on the first and second data (decision) values (see column 7, lines 8-16); and

generating a second received data value (current bit) based on the first and second decision values as disclosed in column 7, lines 8-16 when the input signal is a multi-level signal as disclosed in column 11, lines 14-21, wherein a multi-level signal includes more constituent bits than the binary input signal disclosed in column 7, lines 8-16.

Gitlin et al. does not specifically disclose the decision values are sample values generated using comparators which compare the samples to a threshold value or the received data values are generated based on a mode select signal. However, Gitlin et al. does disclose using comparators to generate the data values which can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Popplewell et al. further discloses sampling an input signal regular intervals and a threshold slicer which selects an ideal sample by comparing sampled values with received thresholds (see Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of Gitlin et al. to compare samples with the thresholds as taught by Popplewell et al. and to use different phase timing for the sampling clocks since Gitlin et al. states that the comparators can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Darabi et al. further discloses generating received radio frequency data values based on a mode selection signal (Fig. 1, element 34, column 3, lines 6-11) which is used to select the operational mode of the receiver. Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since Gitlin et al. discloses the receiver can operate in different modes (see column 11, lines 14-21) to modify the receiver of Gitlin et al. and

Popplewell et al. with the mode selection signal of Darabi et al. to allow the receiver Gitlin et al. and Popplewell et al. to increase the adaptability of the receiver by allowing the receiver to operate in different modes and to allow the receiver to be designed to meet the performance requirements of multiple wireless standards (see Darabi et al., column 3, lines 53-55).

Regarding claim 73, Gitlin et al. further discloses operating the receiver using multi-level signaling (column 11, lines 14-21), wherein multi-level signaling includes signals with at least two bits.

Regarding claim 74, Gitlin et al. discloses creating a first received decision (data) value comprising one bit (see column 7, lines 8-16).

Regarding claim 76, Gitlin et al. further discloses generating a third data value (Fig. 5, Cj) having either the first state or the second state (0 or 1) according to whether the input data signal exceeds a third threshold level (V3).

Regarding claims 80 and 81, Popplewell et al. further discloses generating samples at regular intervals (see Abstract) in response to a rising edge transition of a clock signal (see column 3, lines 27-30). It would have been obvious to include this feature since Gitlin et al. states that the use of (sampling) clocks with different phase timings generates a comparative threshold which would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Regarding claim 82, Gitlin et al. discloses generating the first received (bit) data value comprises selecting either the first data (decision) value or the second data value to be the received bit decision value (column 7, lines 8-16).

Regarding claim 83, Gitlin et al. discloses selecting either the first (decision) data value or the second data value to be the received (bit) data value (column 7, lines 8-16) comprises selecting either the first value or the second value according to whether a third sample (aj-1) is in the first state (0) or the second state (1).

Regarding claim 84, Gitlin et al. discloses the third data value (aj-1) is generated immediately prior to the first and second values (column 7, lines 8-16).

Regarding claim 85, Gitlin et al. discloses generating first and second thresholds (V1 and V2) using a reference signal generator (Fig. 4, block 438, column 6, lines 57-64).

Regarding claim 86, Gitlin et al. further discloses generating (updating) a first pair of thresholds using one mode which incorporates a rate or change of distortion (see column 5, lines 23-35) and also updating thresholds using different mode of operation which involves an analog value of an error signal (column 11, lines 23-28). Therefore, it would have been obvious to one skilled in the art to allow selection of a mode of operation as described by Darabi et al. (see column 3, lines 6-11) to allow the devcie to meet multiple performance requirements (see Darabi et al., column 3, lines 53-55).

Regarding claim 87, Gitlin et al. further discloses the threshold levels are generated based upon the difference generated at subtracter 436 of Fig. 4 between signal levels (swings) of the input signals and the reference voltage levels (V1 and V2), see also column 5, lines 23-35).

Regarding claim 88, Gitlin et al. discloses generating threshold levels based on a rate of change of distortion (wherein intersymbol interference is distortion) in a channel (see column 5, lines 23-35).

Regarding claim 106, Gitlin et al. discloses detector/non-linear canceller which can be implemented as an integrated circuit device (Figs. 4 and 5, column 11, lines 48-50) comprising:

a first comparator circuit (Fig. 4, block 411, column 6, line 64-column 7, line 10) to compare an input data signal with a threshold, the first comparator circuit being configured to generate a decision value having either a first state or a second state (0 or 1) according to whether the input data signal, when compared, is above or below a selected threshold level (V1); and

a reference signal generator (Fig. 4, block 438) representing a threshold generating circuit to establish the selected threshold level (column 6, lines 57-64) within the first comparator circuit, the threshold generating circuit establishing the selected threshold level at a first threshold level using a first operation mode involving a rate of change of distortion (column 5, lines 25-35) and establishing the selected threshold using a second mode of operation involving the use of an analog error signal (see column 11, lines 22-27).

Gitlin et al. does not specifically disclose the generateg decision values are sample values generated using comparators which compare the samples to a threshold value or the threshold generating operation modes are selected using a mode select signal. However, Gitlin et al. does disclose using comparators to generate the data values which can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well (column 9, lines 13-20). Popplewell et al. further discloses sampling an input signal regular intervals and a threshold slicer which selects an ideal sample by comparing sampled values with received thresholds (see Abstract). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of Gitlin et al. to

compare samples with the thresholds as taught by Popplewell et al. and to use different phase timing for the sampling clocks since Gitlin et al. states that the comparators can use clocks with different phase timings so that the comparative threshold would depend not only on the previous bits but also the sample time as well, allowing for better distortion compensation (column 9, lines 13-20).

Darabi et al. further discloses generating received radio frequency data values based on a mode selection signal (Fig. 1, element 34, column 3, lines 6-11) which is used to select the operational mode of the receiver. Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since Gitlin et al. discloses the threshold generating circuit can operate in different modes (see column 11, lines 23-28) to modify the receiver of Gitlin et al. and Popplewell et al. with the mode selection signal of Darabi et al. to increase the adaptability of the device by being able to choose between the different operational modes and to allow the receiver to be designed to meet the performance requirements of multiple wireless standards (see Darabi et al., column 3, lines 53-55).

Regarding claim 107, Gitlin et al. further discloses the device can operate in a binary reception mode or a multi-level signal reception mode (column 11, lines 14-21). Therefore, it would have been obvious to one skilled in art at the time the invention was made to allow selection between two different modes of operation in a receiver as described by Darabi et al. (see column 3, lines 6-11) to increase the adaptability of the device by being able to choose between the different operational modes and to allow the receiver to be designed to meet the performance requirements of multiple wireless standards (see Darabi et al., column 3, lines 53-55).

Regarding claim 108, Popplewell et al. further discloses a phase locked loop (Fig. 1) representing a clock recovery circuit to generate a first clock (oscillator) signal that transitions (samples) on the frequency of interest of the input data signal (column 1, lines 28-36). It would have been obvious to include this feature since Popplewell et al. states correct alignment of the clock (oscillator) signal is critical in performing correct data recovery.

Regarding claim 109, Popplewell et al. further discloses a phase detector (Fig. 1, block 5) to receive a sample (column 3, lines 27-35) represented by a digital value and configured to align (advance or retard) the phase of the clock signal (Fig. 1, element 15, see column 1, lines 33-38) based on the phase error associated with the sample value which is used to phase align the clock signal using the oscillator (VFO) (see column 3, lines 31-43). It would have been obvious to include this feature since Popplewell et al. states correct alignment of the clock (oscillator) signal is critical in performing correct data recovery.

9. Claim 145 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071) as applied to claim 144, and in further view of Min et al. (U. S. Patent No. 5, 402, 378).

Regarding claim 145, Gitlin et al. and Popplewell et al. do not disclose outputting an equalizing signal onto the electric signal conductor during each one of the transmission intervals to reduce inter-symbol interference resulting from data values transmitted prior to the current data values.

However, Min et al. disclsoes an equalizer driver (Fig. 4, block 70) to provide an equalizer signal to a bit line to increase the amplitude of the bit line (to Vcc level) as disclosed in column 3, lines 59-67. Therefore, it would have been obvious to one skilled in the art at the time

the invention was made to modify the method of Gitlin et al. and Popplewell et al. with the equalization signal of Min et al. to adjust the amplitude level of the conductor (line) to a sufficient amplitude level (wherein the amplitude level can be decreased by previous interference) to allow the proper sensing of data transmitted on the line (see Min et al., column 4, lines 48-53).

10. Claims 146 and 147 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (U. S. Patent No. 5, 1941, 462) in view of Popplewell et al. (U. S. Patent No. 6, 304, 071) in view of Min et al. (U. S. Patent No. 5, 402, 378), as applied to claim 145, and in further view of Sullivan (U. S. Patent No. 3, 582, 879).

Regarding claims 146 and 147, Min et al. further discloses generating the equalization signal with a driver (Fig. 4, block 70) which uses a weighting signal (Vpp) to control the drive strength of the driver (see column 3, lines 61-67). Gitlin et al., Popplewell et al., and Min et al. do not disclose generating an equalizing signal according to data values transmitted prior to current data values.

However, Sullivan discloses equalizing a signal with previously existing equalization control signals (column 2, lines 65-72), wherein the previously existing equalization control signal are generate using previously (preliminary) equalized digital signals (see column 3, lines 20-36). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the equalizer of Gitlin et al., Popplewell et al., and Min et al to use previous equalization signals generated from previously transmitted values as disclosed by Sullivan since Sullivan states this method compensates for channel induced distortion (column 2, lines 65-72).

Allowable Subject Matter

11. Claims 53-71 are allowable over prior art references because related references do not disclose comparing first and second samples to first and second thresholds, wherein in a first mode based on the comparison, outputting a most significant bit and a least significant bit, and in a second mode of operation, based on the comparison, outputting the first sample or the second sample.

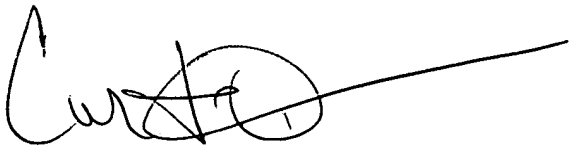
12. Claim 20-29, 41, 46, 47, 75, and 77-79 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Curtis Odom
July 10, 2006